ABSTRACT

A jitter-less phase detector in a clock recovery circuit is disclosed. A first control signal generating circuit generates a first control signal by inverting and delaying input data signals through half clock. A second control signal generating circuit generates a high level second control signal when the data signal changes. A phase comparator generates an up signal having a high-level from the falling edge of the first control signal to the falling edge of the second control signal, and generates a down signal having a high-level from the falling edge of the second control signal to the falling edge of the first control signal, so as to control a pair of current sources to selectively discharge and charge a capacitor.